CLAIMS

What is claimed is:

1. A microcomputer having an on-chip programming capability, the microcomputer comprises:

an embedded flash memory unit that is partitioned into at least two blocks including:

a loader block for storing a loader program; and

a user block, having the same starting address as the loader block, for storing at least one application program;

a microprocessor unit coupled to the embedded flash memory unit, the microprocessor unit including a timer capable of generating an interrupt signal when a preset time period elapses;

a register set for temporarily storing the data to be programmed into the user block of the embedded flash memory unit; and

a bus multiplexer coupled between the microprocessor unit, the embedded flash memory unit, and the register set, in order to selectively connect the embedded flash memory unit to either the microprocessor unit or the register set in response to a bus selection signal issued by the microprocessor unit;

wherein

when performing a data reprogramming process, the microprocessor unit selects the loader block of the embedded flash memory unit as the active block while instructing the bus multiplexer to connect the loader block of the embedded flash memory unit to the microprocessor unit, allowing the microprocessor unit to fetch and execute the loader program stored in the loader block of the embedded flash memory unit;

25

Copied from 09984683 on 12/06/2010

when performing the data reprogramming process, ~~the~~ externally received data are first transferred to and temporarily stored in the register set and the time period required to write one block of data into the user block of the embedded flash memory unit is set to the timer in the microprocessor unit; and

wherein

when the microprocessor unit subsequently is switched to an idle mode and selects the user block of the embedded flash memory unit as the active block, it also instructs the bus multiplexer to connect the user block of the embedded flash memory unit to the register set, allowing the data currently stored in the register set to be transferred to and written into the user block of the embedded flash memory unit; and

when the preset period of time elapses and the timer generates the interrupt signal, the interrupt signal causes the microprocessor unit to wake up from the idle mode and resume operation.

2. The microcomputer of claim 1, wherein the embedded flash memory unit further includes an I/O circuit that is shared by both the loader block and the user block of the embedded flash memory unit for I/O functions.

3. The microcomputer of claim 2, wherein the microprocessor unit issues a memory selection signal to the embedded flash memory unit to select either the loader block or the user block of the embedded flash memory unit as the active block connected to the I/O circuit.

4. The microcomputer of claim 3, wherein the microprocessor unit further includes an I/O port for receiving the data to be programmed into the user block of the embedded flash memory unit.

Copied from 09984683 on 12/06/2010

5. The microcomputer of claim 4, wherein the register set includes:

a data register for storing the data to be programmed into the user block of the embedded flash memory unit;

an address register for storing the associated addresses of the data to be programmed into the user block of the embedded flash memory unit; and

a control register for storing the control instructions related to the programming of the data into the user block of the embedded flash memory unit.

6. The microcomputer of claim 5, wherein the microprocessor unit operates in a programming mode and an execution mode, such that when in the programming mode, the microprocessor unit fetches and executes the loader program stored in the loader block of the embedded flash memory unit, and when in the execution mode, the microprocessor unit fetches and executes the application program stored in the user block of the embedded flash memory unit.

7. The microcomputer of claim 6, wherein when the microprocessor unit operates in the programming mode, the microprocessor unit issues a memory selection signal to the embedded flash memory unit to select the loader block as the active block, and also issues a bus selection signal to the bus multiplexer causing the bus multiplexer to connect the active block of the embedded flash memory unit to the microprocessor unit, allowing the microprocessor unit to execute the loader program stored in the loader block of the embedded flash memory unit.

8. The microcomputer of claim 7, wherein when the microprocessor unit operates in the execution mode, the microprocessor unit issues a memory selection signal to the embedded flash memory unit to select the user block as the active block, and also issues a bus selection signal to the bus multiplexer to cause the bus multiplexer to connect the

Copied from 09984683 on 12/06/2010

active block of the embedded flash memory unit to the microprocessor unit, allowing the microprocessor unit to execute the application program stored in the user block of the embedded flash memory unit.

9. The microcomputer of claim 8, wherein when the microprocessor unit operates in the idle mode, if the control instruction stored in the control register is set to programming mode, the data currently stored in the data register are transferred to and written into the user block of the embedded flash memory unit at locations specified by the address values stored in the address register.

10. The microcomputer of claim 9, wherein the microprocessor unit, prior to entering into the idle mode, enables an interrupt function that allows the microprocessor unit to be interrupted by the interrupt signal generated by the timer.

11. The microcomputer of claim 10, wherein the microprocessor unit, prior to entering into the idle mode, checks the time period required to write the new data into the user block of the embedded flash memory unit and then set the timer accordingly.

12. The microcomputer of claim 11, wherein when the microprocessor unit operates in the execution mode, it enters the idle mode after the interrupt function is enabled and the timer is set, and when the timer reaches the preset time, the timer generates an interrupt signal to wake up the microprocessor unit from the idle mode and cause the microprocessor to enter the programming mode.

13. The microcomputer of claim 12, wherein when the microprocessor unit operates in the programming mode, the microprocessor unit is switched into the execution mode after the instruction to enter the execution mode is set and the microprocessor unit is restarted.

Copied from 09984683 on 12/06/2010

14. A microcomputer having an on-chip programming capability, which comprises:

an embedded flash memory unit that is partitioned into at least two blocks including:

a loader block for storing a loader program; and

a user block, having a starting address following immediately after the last address of the loader block, for storing at least one application program;

a microprocessor unit coupled to the embedded flash memory unit, the microprocessor unit including a timer capable of generating an interrupt signal when a preset time period elapses after the timer is started;

a register set for temporarily storing the data to be programmed into the user block of the embedded flash memory unit; and

a bus multiplexer coupled between the microprocessor unit, the embedded flash memory unit, and the register set, for selectively connecting the embedded flash memory unit to either the microprocessor unit or the register set in response to a bus selection signal issued by the microprocessor unit;

wherein

when performing a data reprogramming process, the microprocessor unit selects the loader block of the embedded flash memory unit as the active block and meanwhile instructs the bus multiplexer to connect the loader block of the embedded flash memory unit to the microprocessor unit, allowing the microprocessor unit to fetch and execute the loader program stored in the loader block of the embedded flash memory unit;

when performing the data reprogramming process, ~~the~~ externally received data are first transferred to and temporarily stored in the register set and the period of time required to

Copied from 09984683 on 12/06/2010

write one block of data into the user block of the embedded flash memory unit is used set to the timer in the microprocessor unit; and

subsequently, the microprocessor unit is switched to idle mode and then selects the user block of the embedded flash memory unit as the active block and meanwhile instructs the bus multiplexer to connect the user block of the embedded flash memory unit to the register set, allowing the data currently stored in the register set to be transferred to and written into the user block of the embedded flash memory unit, while at the time the timer generates an interrupt signal when the preset period of time elapses after the timer is started, and the interrupt signal causes the microprocessor unit to wake up from the idle mode and resume operation.

15. The microcomputer of claim 14, wherein the embedded flash memory unit further includes:

an I/O circuit which is shared by both the loader block and the user block of the embedded flash memory unit for I/O functions.

16. The microcomputer of claim 15, wherein the microprocessor unit further includes:

an I/O port for receiving the data to be programmed into the user block of the embedded flash memory unit.

17. The microcomputer of claim 16, wherein the register set includes:

a data register for storing the data to be programmed into the user block of the embedded flash memory unit;

an address register for storing the associated addresses of the data to be programmed into the user block of the embedded flash memory unit; and

Copied from 09984683 on 12/06/2010

a control register for storing the control instructions related to the programming of the data into the user block of the embedded flash memory unit.

18. The microcomputer of claim 17, wherein the microprocessor unit operates in a programming mode and an execution mode, such that when in the programming mode, the microprocessor unit fetches and executes the loader program stored in the loader block of the embedded flash memory unit, and when in the execution mode, the microprocessor unit fetches and executes the application program stored in the user block of the embedded flash memory unit.

19. The microcomputer of claim 18, wherein when the microprocessor unit operates in the programming mode or the execution mode, the microprocessor unit issues a bus selection signal to the bus multiplexer to cause the bus multiplexer to connect the currently addressed block of the embedded flash memory unit to the microprocessor unit.

20. The microcomputer of claim 19, wherein when the microprocessor unit operates in the idle mode, if the control instruction stored in the control register is set to programming mode, the data currently stored in the data register are transferred to and written into the user block of the embedded flash memory unit at locations specified by the address values stored in the address register.

21. The microcomputer of claim 20, wherein the microprocessor unit, prior to entering into the idle mode, enables an interrupt function that allows the microprocessor unit to be interrupted by the interrupt signal generated by the timer.

22. The microcomputer of claim 21, wherein the microprocessor unit, prior to entering the idle mode, checks the period of time required to write the new data into the user block of the embedded flash memory unit and then set the timer accordingly.

Copied from 09984683 on 12/06/2010

23. The microcomputer of claim 22, wherein when the microprocessor unit operates in the execution mode, it enters into the idle mode after the interrupt function is enabled and the timer is set, and when the timer reaches the preset time, the timer generates an interrupt signal to wake up the microprocessor unit from the idle mode and the microprocessor enter the programming mode.

24. The microcomputer of claim 23, wherein when the microprocessor unit operates in the programming mode, the microprocessor unit is switched into the execution mode after the instruction to enter the execution mode is set and the microprocessor unit is restarted.

25. A method for use on a microcomputer having a microprocessor unit ~~and~~ , and a register set an embedded flash memory unit to perform an on-chip programming process for programming a set of new data into the embedded flash memory unit, the method comprising the steps of:

(1) partitioning the embedded flash memory unit into a loader block for storing a loader program and a user block for storing at least one application program;

(2) switching the microprocessor unit to ~~programming mode;~~

(3) executing the loader program stored in the loader block of the embedded flash memory unit by the microprocessor unit;

(4) setting parameters related to the programming of the new data into the embedded flash memory unit;

(5) ~~receiving one block of the new data;~~

(6) writing the currently received block of data into the user block of the ~~microprocessor unit; and~~

Copied from 09984683 on 12/06/2010

(10) checking whether all the blocks of the new data have been programmed into the user block of the embedded flash memory unit; if not, returning to the step (5).

26 The method of claim 25, further comprising the step of checking whether a request for data reprogramming process is received; if not, instructing the microprocessor unit to execute the application program stored in the user block of the embedded flash memory unit.

27. The method of claim 26, wherein the step (5) comprises the substep of writing the new data and the address values associated with the new data into a register set.

28. The method of claim 27, wherein the new data are received first via an I/O port of the microprocessor unit and then transferred to the register set.

29. The method of claim 28, further comprising the steps of:

checking the period of time required to program one block of data into the user block of the microprocessor unit; and

setting a timer in the microprocessor unit with the period of time, the timer being capable of generating an interrupt signal to the microprocessor unit when the preset period of time elapses after the timer is started.

30. The method of claim 29, wherein the step (2) of switching the microprocessor unit to the programming mode includes the substeps of:

initializing the programming mode;

enabling the interrupt function of the microprocessor unit;

setting the timer with the period of time required to program one block of data into the user block of the microprocessor unit, the timer being capable of generating an interrupt signal when a preset period of time elapses after the timer is started;

starting the timer;

Copied from 09984683 on 12/06/2010

switching the microprocessor unit into idle mode;

upon receiving the interrupt signal from the timer, waking up the microprocessor unit from the idle mode;

stopping the timer; and

disabling the interrupt function of the microprocessor unit.

31. The method of claim 30, further comprising, prior to the step (4) of setting parameters, the step of checking whether the programming mode is readily entered, and if it is not, reinitializing the programming mode.

32. The method of claim 31, wherein the step (6) of writing data includes the substeps of:

enabling the interrupt function of the microprocessor unit;

starting the timer;

switching the microprocessor unit into idle mode;

transferring the data currently stored in the register set to the user block of the embedded flash memory unit, and then writing these data into the user block of the embedded flash memory unit;

upon receiving the interrupt signal from the timer, waking up the microprocessor unit from the idle mode;

stopping the timer; and

disabling the interrupt function of the microprocessor unit.

33. The method of claim 32, further comprising the step of checking whether the data reprogramming process is completed; if yes, setting the instruction to enter the execution mode, and then restarting the microprocessor unit.

* * * * *

34

Copied from 09984683 on 12/06/2010